In The Claims:

1-15 (cancelled)

16. (New) A method of determining proper process time of chemical mechanical polishing, the method comprising:

forming a film on a wafer having at least one device region and at least one test region;

calculating a first pattern density of the device region to determine a second pattern density of the test region such that the second pattern density is substantially compatible with the first pattern density;

patterning the film on the wafer to form a first pattern, having the first pattern density, on the device region and a second pattern, having the second pattern density, on the test region to form dummy structures on the substrate; and

polishing the film on the wafer by chemical mechanical polishing until a thickness of the film on the test region is zero.

17. (New) The method of claim 16, wherein the second pattern density is less than 10 times of the first pattern density.

18. (New) The method of claim 16, wherein the second pattern density is the same as the first pattern density.

19. (New) A method of forming shallow trench isolation, the method comprising:

forming a first dielectric layer on a wafer having at least one device region and at least one test region;

etching the first dielectric layer and the wafer to form at least one trench on the device region;

forming a second dielectric layer on the wafer and in the trench to fill the trench;

calculating a first pattern density of the device region to determine a second pattern density of the test region such that the second pattern density is substantially compatible with the first pattern density;

etching the second dielectric layer on the wafer to form a first pattern, having the first pattern density, on the device region and a second pattern, having the second pattern density, on the test region until the first dielectric layer is exposed, and transforming the second dielectric layer to dummy structures on the substrate; and

polishing the second dielectric layer on the wafer by chemical mechanical polishing until a thickness of the second dielectric layer on the test region is zero to form shallow trench isolation in the trench.

20. (New) The method of claim 19, wherein the second pattern density is less than 10 times of the first pattern density.

21. (New) The method of claim 19, wherein the second pattern density is the same as the first pattern density.

22. (New) The method of claim 19, wherein the sizes of the dummy structures are about the same.

23. (New) The method of claim 19, wherein the first pattern density on the device region is obtained by calculating a ratio of the area of the dummy structures to the total area of the device region.

24. (New) The method of claim 19, wherein the first dielectric layer comprises a silicon nitride layer as a stop layer in the chemical mechanical polishing process.

25. (New) The method of claim 19, wherein the second dielectric layer comprises a silicon oxide layer formed by high-density plasma CVD.